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Solution-Processed Wide-Bandgap Organic Semiconductor Nanostructures Arrays for Nonvolatile Organic Field-Effect Transistor Memory

Wen Li, Fengning Guo, Haifeng Ling, Hui Liu, Mingdong Yi, Peng Zhang, Wenjun Wang, Linghai Xie,* and Wei Huang**

In this paper, the development of organic field-effect transistor (OFET) memory device based on isolated and ordered nanostructures (NSs) arrays of wide-bandgap (WBG) small-molecule organic semiconductor material [2-(9-(4-(octyloxy)phenyl)-9H-fluoren-2-yl)thiophene]3 (WG_3) is reported. The WG_3 NSs are prepared from phase separation by spin-coating blend solutions of WG_3/trimethylolpropane (TMP), and then introduced as charge storage elements for nonvolatile OFET memory devices. Compared to the OFET memory device with smooth WG_3 film, the device based on WG_3 NSs arrays exhibits significant improvements in memory performance including larger memory window (≈45 V), faster switching speed (≈1 s), stable retention capability (>10^4 s), and reliable switching properties. A quantitative study of the WG_3 NSs morphology reveals that enhanced memory performance is attributed to the improved charge trapping/charge-exciton annihilation efficiency induced by increased contact area between the WG_3 NSs and pentacene layer. This versatile solution-processing approach to preparing WG_3 NSs arrays as charge trapping sites allows for fabrication of high-performance nonvolatile OFET memory devices, which could be applicable to a wide range of WBG organic semiconductor materials.

Owing to the merits of low-cost, nondestructive read-out, good compatibility with flexible substrates, and easily integrated structure, nonvolatile organic field-effect transistor (OFET) memory devices have attracted extensive attention for their potential applications as basic building blocks in a wide range of organic electronics such as radio frequency identification devices, sensors, flexible circuits, and displays.[1–5] To date, much progress has been made in various types of OFET memory devices, such as floating-gate OFET memory, polymer electret OFET memory, and ferroelectric OFET memory.[6–11] However, OFET memory devices are far less mature than their Si counterparts; many issues remain regarding their charge storage capacity, stability, and reliability, limiting their practical applications. For OFET memory devices, charge storage layer has been considered as an important factor dominating charge trapping and detrapping process, which directly affects memory performance.[12–18] Thus, there is a desire to develop an efficient charge storage layer for high-performance OFET memory device.

Previous studies have reported that the OFET memory devices with well-separated and highly ordered charge trapping sites showed better retention capability and higher charge trapping capacity as compared to those using continuous film or disordered nanoparticles (NPs) as charge trapping elements.[6,19–22] For example, Cho and co-workers have demonstrated that charge trap density can be significantly enhanced by vertically engineering multilayered ferritin NP materials as charge-trapping layer in their approach for the applications of OFET memories. More importantly, the obtained memory performance parameters, such as memory window and programing/erasing current ratios, can be precisely controlled by implementing a different number of such charge-trapping layers.[22] Therefore, it is clear that developing isolated and ordered arrays of charge trapping sites is worth the effort for further research and development. Many materials, which are generally metallic conductors and narrow-bandgap (NBG) semiconductors, have been processed into isolated and ordered charge trapping sites, such as metallic NPs (Au, Ag, Al, Pt NPs, etc.),[20,23–25] inorganic materials (MoS_2, carbon materials, etc.),[26,27] organic molecules (C_{60}, [6,6]-phenyl-C61-butyric acid methyl ester (PCBM), CuPc, etc.),[28–31] conjugated polymer NPs,[32] etc. These studies have contributed to the development of OFET memory devices.

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However, one limiting factor is charge loss caused by the narrow bandgap, resulting in data-retention degradation. Wide-bandgap (WBG) organic semiconductor have been widely used in organic light-emitting diodes (OLEDs),[33,34] while they are rarely reported as charge trapping elements in OFET memory devices. Compared to metallic conductors and NBG semiconductors, WBG semiconductors own a high potential barrier, making it ideal for preserving trapped charges, which holds great promise for use in memory devices. Meanwhile, to prolong data retention time and improve charge storage capacity, it would be highly desired to pattern isolated and ordered arrays of WBG organic semiconductor materials as charge trapping sites for OFET memory devices. In previous reports, numerous methods have been developed to prepare isolated and ordered charge trapping arrays, such as thermal evaporation,[2,23,24] self-assembly,[6,21,25,35] microcontact printing,[20] synthesis in block copolymer,[19] etc. However, these methods face some issues in practical application including high cost, low efficiency, and complex manufacturing process. Therefore, preparing well-separated and ordered charge trapping arrays via inexpensive and simple solution process remains challenging.

Solution process is the most promising approach for commercial manufacturing owing to its low cost, as well as good compatibility with large-area and flexible substrates.[36,37] As a simple solution-processing method, spin-coating is a ubiquitous technique throughout the fields of science and engineering, where it is applied for depositing thin films onto either rigid or flexible substrates for a wide variety of applications. Spinning blends of different materials may result in phase separation, depending on materials, concentration, solvent, substrate, temperature, as well as film deposition process.[38–40] By tuning these relevant parameters, many possible morphologies can be made from the phase separation. Various phase-separated morphologies have been applied in organic electronics, such as OFETs, OLEDs, organic photovoltaic solar cells (OPVs), etc., to improve device performance.[41–44] Motivated by the previous research in phase-separated microstructures, we are interested in developing isolated charge trapping sites using WBG organic semiconductor materials by phase separation from spin-coating blend solutions.

In this work, we report a simple approach to developing WBG small-molecule organic semiconductor material [2-(9-(4-(octyloxy)phenyl)-9H-fluoren-2-yl)thiophene]3 (WG_3) nanostructures (NSs) arrays by spin-coating blend solutions of WG_3/(trimethylolpropane) (TMP). The WG_3 NSs exhibit isolated and well-ordered distribution as a result of phase separation. By employing the WG_3 NSs arrays as charge trapping sites for pentacene-based OFET memory devices, memory characteristics are significantly improved compared to those of the OFET memory device using smooth WG_3 film as charge storage layer. A quantitative study of the WG_3 NSs morphology is carried out using MATLAB to investigate the reason for the enhanced memory performance. Furthermore, operational mechanisms for the OFET memory devices are discussed.

Schematic illustration of the process for forming WG_3 NSs arrays is shown in **Figure 1**a. It is known that most small molecules face difficulty in solution processability, while alkyl chains in WG_3 make it able to have excellent solubility in toluene. The WG_3 NSs arrays were fabricated by spin-coating from toluene solutions of a mixture of WG_3/TMP = 1:5 onto the SiO_2 substrates. It has been demonstrated that surface energy plays an important role in controlling the process of phase separation in

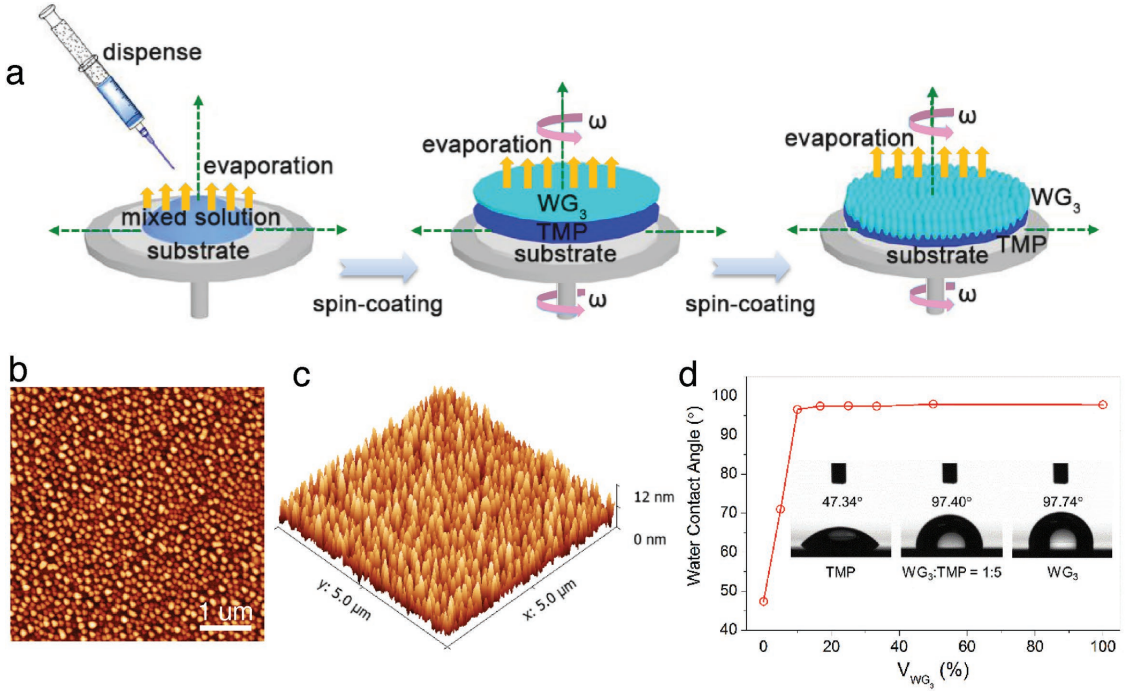

Figure 1. a) Schematic illustration of the process for forming WG_3 NSs arrays. b) 2D and c) 3D AFM images of WG_3 NSs. d) Water contact angles as a function of WG_3 ratio in the blends. Insets: Photographs of a water droplet on pure TMP film, WG_3/TMP (1:5) blended film, and pure WG_3 film.

binary blends and therefore determines the surface morphology of thin film.[38,45] When the WG_3/TMP blend solution dripped onto the hydrophilic SiO_2 substrate, polar material TMP with high surface energy is preferentially deposited on the substrate surface, whereas the WG_3, with low surface energy, forms at the film–air interface, resulting in a vertical stratification. Then the transient stratified layer becomes unstable due to Marangoni-like instability, further leading to a lateral phase separation during solvent evaporation.[39,46] The formation of WG_3 NSs is attributed to the vertical and lateral phase separation caused by the preferential aggregation of TMP at the substrate–film interface and the phase segregation in the film. 2D and 3D atomic force microscopy (AFM) images of the WG_3 NSs arrays are shown in Figure 1b,c, respectively. The WG_3 NSs are found to be uniform with an average height of ≈9 nm. To investigate the structure of phase-separated WG_3, the sectional view from the location indicated by line in the AFM image (Figure S1a, Supporting Information) was obtained, as shown in Figure S1b (Supporting Information). It reveals the nanocolumn-like structures of phase-separated WG_3. In addition, height histogram was extracted from the AFM data to further study the distribution of WG_3 NSs, as shown in Figure S1c (Supporting Information). Two peaks were observed in the WG_3/TMP layer, indicating the presence of two distinct types of surface topographies. The first sharp peak is centered at ≈2.7 nm, corresponding to the height of the bottom film among WG_3 NSs; while the second peak is centered at ≈8 nm, which agrees well with the height of WG_3 NSs. These results suggest that the phase-separated WG_3 NSs are isolated with relatively uniform height. To further confirm the surface composition of the blended film, water contact angle measurements were performed on the WG_3/TMP blended films containing different WG_3 ratios. Photographs of a water droplet on the corresponding surface are exhibited in the insets in Figure 1d. The water contact angle of WG_3 is 97.74° and that of TMP is 47.34°. Figure 1d shows the water contact angle as a function of the WG_3 ratio in the blends. Note that water contact angle of the WG_3/TMP blended film increases rapidly with the increased WG_3 ratios, and reaching a value of 96.56° at WG_3 ratio of 10%, which is almost the same as the water contact angle of pure WG_3 film. This indicates that the NSs are predominantly composed of WG_3. These results demonstrate that isolated and ordered NSs arrays of WBG small-molecule organic semiconductor have been successfully developed in a versatile, low-cost, low-temperature, and easily accessible approach.

With the WG_3 NSs arrays as charge trapping layer, we studied charge transport and charge storage characteristics of the OFET memory devices. An illustration of the 3D structure for the memory device is shown in **Figure 2**a. The devices were fabricated in bottom-gate/top-contact configuration with p-type pentacene as the active layer. Figure 2b shows the molecular structures and the relative positions of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) energy levels of pentacene and WG_3. WG_3 is a WBG material having a strong hole-trapping property, with HOMO energy level of –5.9 eV and LUMO energy level of –2.1 eV, which were studied by cyclic voltammetry (CV), as illustrated in Figure S2 (Supporting Information). Finally, 60 nm of Cu was thermally evaporated on top of the pentacene layer as the source and drain electrodes. In addition, an OFET utilizing a WG_3 film as charge trapping layer (denoted as WG_3 film device) was also fabricated as a reference device to gain a better understanding of the effect of the WG_3 NSs on device performance. The continuous and smooth WG_3 thin film was formed by spin-coating from the homo-WG_3 solution on the SiO_2 substrate, as characterized by AFM in Figure S3 (Supporting Information). The representative output and transfer characteristics of the OFET memory device using WG_3 NSs arrays as charge trapping sites (denoted as WG_3 NSs device) and the WG_3 film device are shown in Figure S4 (Supporting Information). Both devices showed typical p-type field-effect transistor behaviors. The WG_3 NSs device exhibited a mobility (μ) of 0.33 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage (V_{TH}) of –10.58 V, and an ON/OFF current ratio of 10^6, and the WG_3 film device exhibited a μ of 0.79 $cm^2\ V^{-1}\ s^{-1}$, a V_{TH} of –11.84 V, and an ON/OFF current ratio of 10^4, as summarized in Table S1 (Supporting Information). Although there is a decrease in mobility of the WG_3 NSs device, the WG_3 NSs appear to be no significant damage to the hole transport in the conductive channel in the WG_3 NSs device, providing the potential for use in high-performance OFET memory device. Figure S5a,b (Supporting Information) shows the AFM images of 50 nm thick pentacene films obtained on the WG_3 NSs and the WG_3 film, respectively. The AFM measurements indicate that the lower mobility of the WG_3 NSs device was caused by the smaller pentacene grains grown on the relatively rough WG_3 NSs than that grown on smooth WG_3 film.[47,48] Moreover, it is worth noting that the ON/OFF current ratio of the WG_3 NSs device was two orders of magnitude higher than that of the WG_3 film device, which is favorable to obtain a stable and reliable memory device.

To investigate the charge storage characteristics of the WG_3 NSs device, the shifts in the transfer curves were measured, as shown in Figure 2c. When a negative gate bias (V_G) of –100 V was applied to the WG_3 NSs device for 1 s, the transfer curve of the device shifted from its initial position toward the negative-voltage direction and then steadily sustained at the shifted position (defined as the programmed state), indicating that holes trapping occurred in the device. It is interesting to note that in the dark condition the electrical voltage bias could not overwrite the memory device even a high positive voltage of 180 V was applied (Figure S6a, Supporting Information). This is ascribed to a lack of mobile electrons in pentacene in the ambient condition. Previous studies demonstrated that light illumination could generate excitons in the semiconductor layer of OFET memory devices, which can assist the programming/erasing operation with or without external voltage bias.[9,49,50] Therefore, in the erasing process we utilized a white light with light intensity of about 5 mW cm^{-2} to illuminate the memory device. It was found that the transfer curve shifted back to its initial position (defined as the erased state) after the WG_3 NSs device was illuminated for 1 s. Memory window (ΔV_{TH}) is an important parameter for memory devices, which is defined as the difference between V_{TH} in the programmed and the erased states. ΔV_{TH} of the WG_3 NSs device is about 44.8 V, and the corresponding charge trapping density (Δn) in this memory device is estimated to be 2.97×10^{12} cm^{-2} using the equation $\Delta n = \Delta V_{TH} \cdot C_i / e$, where C_i is the capacitance per unit area of the dielectric layer and e is the elementary charge. In addition, to

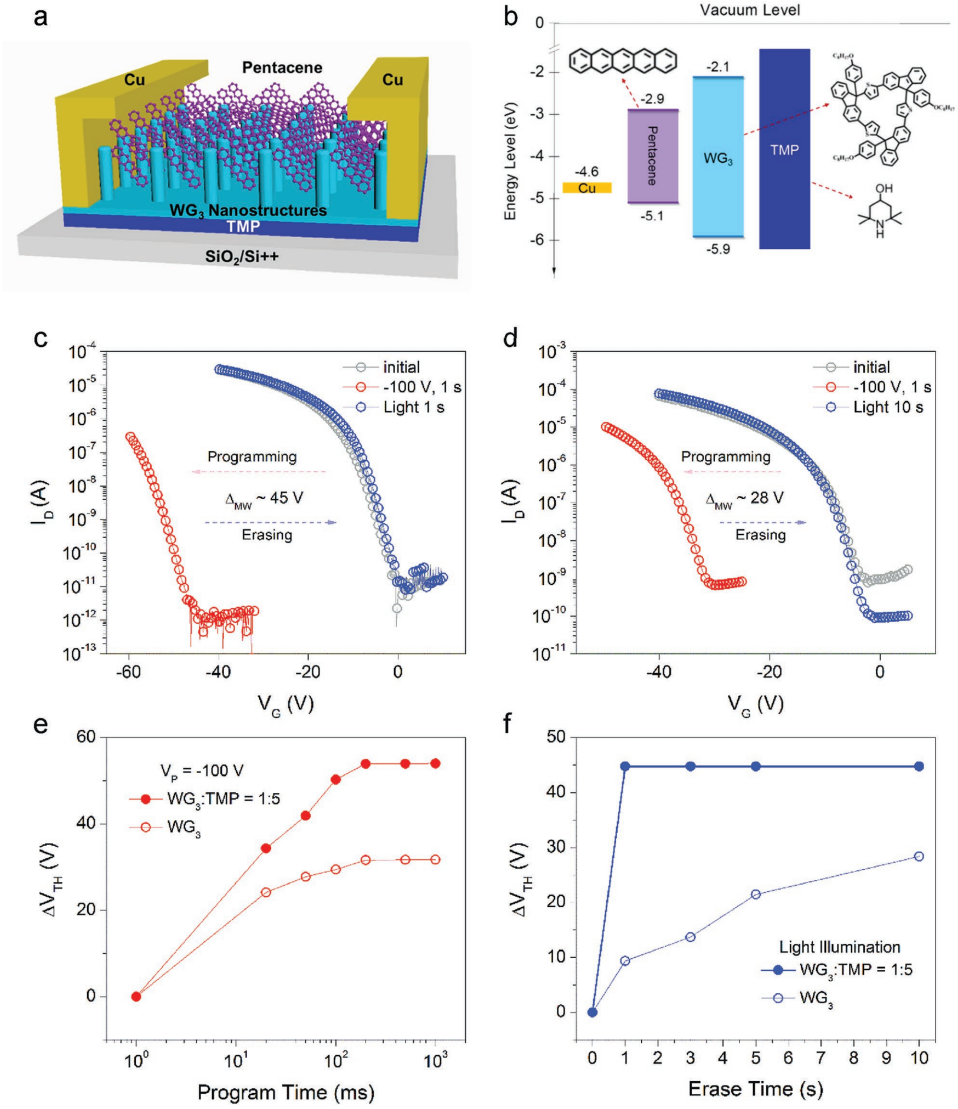

Figure 2. a) Schematic illustration of pentacene-based OFET memory device in bottom-gate/top-contact configuration. b) Energy level diagram and chemical structures of pentacene, WG_3, and TMP. Transfer characteristics obtained under dark after programming and erasing operations for OFET memory devices based on c) WG_3 NSs and d) WG_3 film, with source–drain voltage (V_D) kept at –30 V. For the programming process, both devices were biased at the same V_G of –100 V for 1 s. For the erasing process, white light, with wavelength of 410–800 nm and intensity of 5 mW cm^{-2}, illuminated directly from the top of the devices. WG_3 NSs device was illuminated for 1 s, while WG_3 film device was illuminated for 10 s. V_D = 0 V in both the programming and erasing processes. Variation in V_{TH} as a function of e) program time and f) erase time, respectively, for both WG_3 NSs and WG_3 film devices. V_G = –100 V was applied as the programming voltage, and the same light source was used during the erasing operation.

identify the role of TMP in the memory device, the electrical characteristics of OFET with a single TMP layer were also measured, as shown in Figure S7 (Supporting Information). The OFET with a TMP layer showed negligible shift in transfer curves under a negative gate voltage of –100 V, indicating that the WBG organic semiconductor WG_3 is responsible for the charge storage in the memory device. To further study the effect of the WG_3 NSs on the charge storage, the shifts in the transfer curves of the WG_3 film device were also investigated, as shown in Figure 2d. As in WG_3 NSs device, the WG_3 film device also exhibited electrically inerasable characteristics under dark (Figure S6b, Supporting Information). After a programming voltage of –100 V was applied for 1 s and followed by a light illumination (5 mW cm^{-2} for 10 s), the WG_3 film device exhibited a window width of 27.6 V with a corresponding Δn of 1.83×10^{12} cm^{-2}, which were much smaller than those of the WG_3 NSs device. The results demonstrate that the isolated and ordered WG_3 NSs arrays effectively enhance the charge trapping capacity of the memory device. Moreover, it is interesting to note that in the light-erasing process when the WG_3 film device was illuminated by light for 1 s, the transfer curve shifted back to the initial state by only ≈33%, and could completely return to the initial state until the device was illuminated for 10 s (see Figure S8, Supporting Information). To further study the role of the WG_3 NSs arrays in the charge trapping/charge-exciton annihilation process, the variations in V_{TH} as a function

of programming/erasing durations were characterized in both the WG_3 NSs and WG_3 film devices, as depicted in Figure 2e,f. Here, ΔV_P and ΔV_E denote the variations in V_{TH} in the programming and erasing processes, respectively. As shown in Figure 2e, in the electric-programming process, when the programming pulse width was 20 ms, substantial increases in ΔV_P of both the WG_3 NSs and WG_3 film devices were observed, and the ΔV_P gradually increased and eventually became saturated with the increase of programming duration. However, the WG_3 NSs device showed a larger ΔV_P in contrast to the WG_3 film device under the same programming condition, indicating a higher charge trapping capacity. In the light-erasing process (Figure 2f), ΔV_E of the WG_3 NSs device increased dramatically and reached saturation when the device was illuminated for only 1 s, while the WG_3 film device saw a slow and slight increase in ΔV_E as the illumination time increased. The results demonstrate that utilizing isolated and ordered WG_3 NSs as charge trapping sites is an effective strategy to improve the efficiency of the charge trapping/charge-exciton annihilation.

Data retention characteristics and device switching capability were investigated to evaluate the stability and reliability of the memory devices. The WG_3 NSs device and the WG_3 film device were subjected to the same bias conditions to set the programmed and erased states as shown in Figure 2c,d, respectively. The retention capability of the WG_3 NSs device was found to be well preserved with a high on/off current ratio of 10^5 after 10^4 s (see **Figure 3**a). Further extending the fitting curve, the retention time could exceed five years with an on/off current ratio over 10, as shown in Figure S9 (Supporting Information). In comparison, obvious degradation was observed in the programmed state of the WG_3 film device, leading to a significant reduction in the on/off current ratio from 10^4 to 10^2 in 10^4 s, as shown in Figure 3b. A series of programming ($V_G = -100$ V, $V_D = 0$ V, under dark), reading ($V_G = -25$ V, $V_D = -30$ V, under dark), and erasing ($V_G = 0$ V, $V_D = 0$ V, under illumination) operations was applied to characterize the device switching capability. Figure 3c,d illustrates multiple electric-programming/light-erasing switching cycles of the WG_3 NSs device and the WG_3 film device, respectively. Both devices exhibited reversible memory characteristics for 150 program/erase cycles. Compared to the WG_3 film device, the WG_3 NSs device exhibited more stable switching properties. Thus, utilizing WG_3 NSs arrays as the charge trapping sites successfully improved the stability and the reliability of the memory device, which allow for realizing high-performance OFET memory devices.

Quantitative studies in MATLAB were carried out to explore the correlation between the memory performance and the WG_3 NSs morphology. WG_3 and TMP solutions were mixed at different volume ratios from 1:1 to 1:5, and then the blends were spin-coated to form different blended films. AFM measurements were performed to investigate the surface morphologies of the blended films, as shown in Figure 1b,c, and Figure S10a–c (Supporting Information). It was found that WG_3

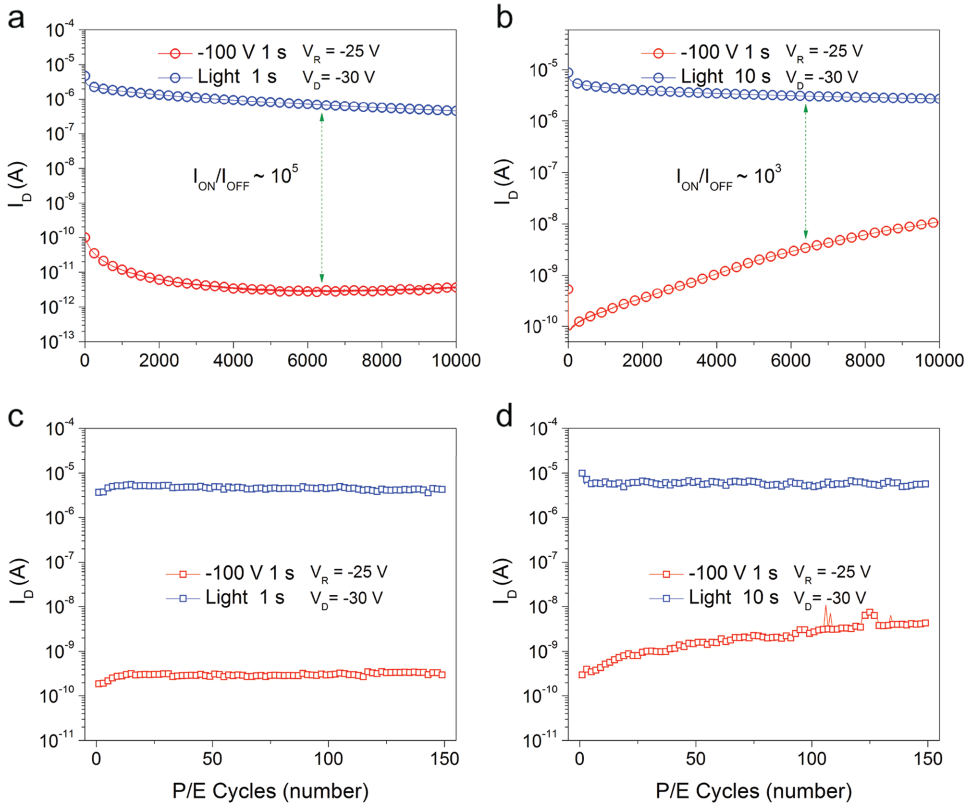

Figure 3. Data retention characteristics of a) WG_3 NSs device and b) WG_3 film device. Program/erase (P/E) cycles of c) WG_3 NSs device and d) WG_3 film device. Program operation: $V_G = -100$ V for 1 s, $V_D = 0$ V, under dark, for both devices; read operation: $V_G = -25$ V, $V_D = -30$ V, under dark, for both devices; erase operation: $V_G = 0$ V, $V_D = 0$ V, light illumination for 1 s for WG_3 NSs device, and light illumination for 10 s for WG_3 film device.

ratio in the blends had a significant impact on determining the domain structures induced by phase separation. With the decrease of the WG_3 ratio in the blends, the domain structures become smaller and more isolated with regular shape, whereas the height of WG_3 NSs appears highly similar in different blended films with an average value of about 10 nm, as confirmed by the 3D AFM images in Figure 1c and Figure S10a–c (Supporting Information). Here, the AFM topography of the WG_3 film was adopted as the standard reference to quantitatively analyze the effect of blend ratios on the morphologies of the blended films. We standardized the color bars in the AFM topographies of the blended films, then used MATLAB to convert the color images to grayscale ones, as shown in **Figure 4**a–d. The proportions of WG_3 NSs (n_p) in different blended films can be simulated and calculated in MATLAB, which were 0 (pure WG_3 film), 0.245734 (WG_3:TMP = 1:5), 0.243747 (WG_3:TMP = 1:3), 0.317749 (WG_3:TMP = 1:2), and 0.484349 (WG_3:TMP = 1:1), respectively. The results indicate that the density of WG_3 NSs increases with the increase of the WG_3 ratio in the blends, which are consistent with the 3D AFM images of the blended films. Furthermore, electrical characteristics of OFETs based on the blended films were also measured (Figure S11, Supporting Information), and the electrical parameters are summarized in Table S1 (Supporting Information). Figure 4e shows the transfer curves of OFETs with WG_3 film or different blended films in the programmed state after applying a gate bias of –100 V for 1 s under dark. It can be seen that more positive V_{TH} was obtained for the device with higher WG_3 ratio. We defined the variation in memory window (Δ_{MW}) as the difference between the memory window of the OFETs with blended films ($\Delta_{TH,\ WG3\ NCs}$) and the memory window of the WG_3 film device ($\Delta_{TH,\ WG3\ film}$). Figure 4f shows Δ_{MW} as a function of n_p, indicating an approximately linear relationship. By linear fitting in MATLAB, the relationship between Δ_{MW} and n_p can be expressed by the following equation with a linear fitting correlation coefficient of 0.93

$$\Delta_{MW} = 101.00591 n_p - 2.73322 \tag{1}$$

As displayed in the 3D AFM image (Figure 1c) and the sectional view of AFM image (Figure S1a, Supporting Information), the WG_3 NSs exhibited nanocolumn-like structure. For simplicity of analysis, we presume that the nanocolumn-like WG_3 NSs in the different blended films have the same height (h) and radius (r). The surface area of the top (S_t), the surface area of the side (S_s), and n_p can be calculated using the following equations

$$S_t = n_p \int_0^r \pi \, dr^2 = n_p \pi r^2 \tag{2}$$

$$S_s = n_p \int_0^r 2\pi h \, dr = n_p 2\pi h r \tag{3}$$

$$n_p = \frac{S_t}{S} \tag{4}$$

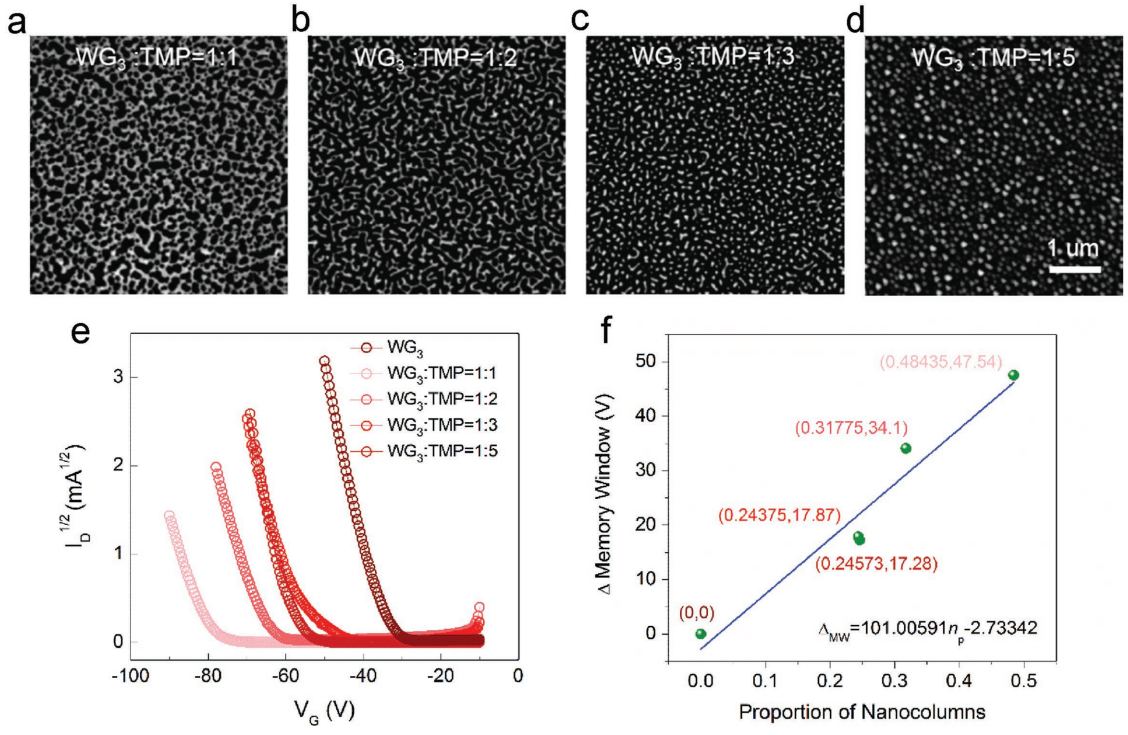

Figure 4. Grayscale images of blended films with WG_3/TMP blend ratio of a) 1:1, b) 1:2, c) 1:3, and d) 1:5, converted from the color AFM images using MATLAB. e) Transfer curves of OFETs with pure WG_3 film or blended films in the programmed state after applying V_G = –100 V for 1 s under dark. f) Variation in memory window (Δ_{MW}) as a function of proportion of WG_3 nanocolumns (n_p) on blended films with different WG_3/TMP blend ratios, where n_p was simulated and calculated in MATLAB. Δ_{MW} and n_p were found to be linearly dependent with a correlation coefficient of 0.93 by linear fitting in MATLAB.

where π is a constant, and S is the surface area of the conductive channel of the OFETs. The relationship between Δ_{MW} and S_s can be extracted from the above equations

$$\Delta_{MW} = 50.502955\frac{r}{hS}S_s - 2.73322 \quad (5)$$

This result indicates that Δ_{MW} is linearly related to S_s. Moreover, S_s is approximately equal to the contact area between the WG_3 NSs and the pentacene film (S_c), because S_t is far smaller and therefore can be neglected with respect to S_s. In this case, it can be concluded that Δ_{MW} and S_c exhibit a practically linear relationship, which impressively demonstrates that the improvement in memory window can be ascribed to the increased contact area between the WG_3 NSs and the pentacene film. Moreover, we also measured the data retention characteristics and switching capability of each device with different WG_3/TMP blend ratio, as shown in Figure S12 (Supporting Information). All the memory devices exhibited reversible and stable switching capabilities, however, the retention properties showed obvious degradation with the increase of WG_3 ratio. This is supposed to originate from the diffusion of trapped charges in the continuous WG_3 domain, resulting in poor retention stabilities. This result reveals that isolated WG_3 NSs as charge trapping sites contribute to stable and reliable memory performance.

Operational mechanisms of the WG_3 NSs device and the WG_3 film device are illustrated in Figure S13 (Supporting Information). As shown in Figure S13a,c (Supporting Information), when the memory devices are subjected to an appropriate negative gate bias in dark condition, holes are injected by tunneling into the WG_3, and steadily trapped by WG_3 due to its strong hole-trapping capability as well as the large energy barrier between the HOMO of pentacene and WG_3. The trapped holes in the WG_3 result in a reduced concentration of holes in the semiconductor channel. Consequently, the transfer curve shifts to the negative-voltage direction, which is the electric-programming process. In the light-erasing process, when the memory devices are illuminated, a large amount of excitons are generated in pentacene and then move to the pentacene/WG_3 interface where charge-exciton annihilation subsequently occurs, resulting in the neutralization of trapped holes in WG_3 (Figure S13b,d, Supporting Information).[49,50] Thus, the transfer curve shifts back to the positive-voltage direction. Interestingly, the energy levels of the WG_3 NSs and the WG_3 film appear to be identical, which indicates the same tunneling barrier with pentacene; however, the memory performance of the WG_3 NSs device is far superior to that of the WG_3 film device. Compared to the WG_3 film, the WG_3 NSs have larger contact area with the pentacene film due to their nanocolumn-like structures, which substantially increases the probability of charge tunneling from the semiconductor channel to the gate dielectric during electric-programming process, and charge-exciton annihilation at pentacene/WG_3 interface during light-erasing process, leading to a remarkable improvement in charge trapping capacity and switching speed of the memory device.[9,51,52] Moreover, the isolated WG_3 NSs structures can effectively suppress the lateral diffusion of the trapped holes among the WG_3 NSs, which enable memory device with high stability and reliability.

In conclusion, the WBG small-molecule organic semiconductor material WG_3 has been successfully processed into isolated and ordered NSs arrays as a result of phase separation by spin-coating blend solutions of WG_3/TMP. We achieved remarkable improvements in memory performance by employing the WG_3 NSs as charge trapping sites for pentacene-based OFET memory device compared to the device using smooth WG_3 film as charge trapping layer. The quantitative study of the WG_3 NSs morphology reveals that enhanced memory performance is attributed to the improved charge trapping/charge-exciton annihilation efficiency induced by increased contact area between the WG_3 NSs and pentacene layer. Meanwhile, the isolated WG_3 NSs structures can effectively suppress the lateral diffusion of the trapped holes in the WG_3, and therefore improve the stability and reliability of the memory device. Our study demonstrates a versatile, low-cost, low-temperature, and easily accessible spin-coating method to form isolated and ordered WG_3 NSs, which could be applicable to fabrication of well-separated and highly ordered arrays of charge trapping sites for high-performance OFET memory devices for promising applications in flexible electronics.

Experimental Section

Fabrication of WG_3 NSs: WG_3 was synthesized by the authors' group, and TMP was purchased from Sigma-Aldrich and used as received. Pure WG_3 and TMP solutions were prepared using toluene (3 mg mL^{-1}). Blend solutions were prepared by mixing the pure WG_3 and TMP solutions in different volume ratios (WG_3:TMP = 1:1, 1:2, 1:3, and 1:5, respectively). The blend solutions were ultrasonically treated for 1 h at room temperature to promote complete dissolution. The blend solutions were spin-coated onto the SiO_2 substrates at a spin speed of 3000 rpm for 30 s. Then the blended films were dried at 80 °C for 30 min in an oven to remove the residual solvent.

Device Preparation: All the OFETs were fabricated in a top-contact and bottom-gate configuration. Heavily doped n-type Si substrates with 300 nm thermally grown silicon dioxide were cleaned in sequence by bath sonication with acetone, isopropanol, and deionized water for 12 min each, and then transferred into an oven at 120 °C for 30 min after dried using a nitrogen gun. For WG_3 NSs device, the WG_3 NSs were prepared by spin-coating from the blend solutions of WG_3/TMP (1:5) onto the SiO_2 substrates. To fabricate reference devices, WG_3 film was formed by spin-coating from pure WG_3 solution in toluene (0.5 mg mL^{-1}), and TMP film was prepared by spin-coating from pure TMP solution in toluene (2.5 mg mL^{-1}). All the solution-processed films were fabricated by spin-coating at the same spin speed of 3000 rpm for 30 s, and then dried at 80 °C for 30 min in an oven. Then pentacene (purchased from Sigma-Aldrich, used without further purification) was thermally deposited with a deposition rate of 0.1 Å s^{-1} under vacuum at a pressure of $\approx 5 \times 10^{-4}$ Pa to form the 50 nm thick film. As a final step, source and drain electrodes of about 60 nm thick copper (Cu) were thermally evaporated through a shadow mask. The channel length (L) and width (W) of the devices were 100 and 2000 µm, respectively.

Characterization: The surface morphologies of different films were obtained with a Bruker Dimension Icon AFM operated in tapping mode (Bruker Sb/Si probe tip with a resonant frequency 320 kHz and the spring constant 42 N m^{-1}) at room temperature. Water contact angles were characterized by using a Krüss DSA-20 contact angle measurement system. The electrical characteristics of the OFETs were measured by using a Keithley 4200 SCS semiconductor parameter analyzer in a shielding box under ambient conditions. Commercial LED, with a wavelength of 410–800 nm and an intensity of 5 mW cm^{-2}, was illuminated directly from the top of the devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

nanostructures arrays, nonvolatile memory, phase separation, solution process, wide-bandgap organic semiconductors

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